Document

Select the documents you wish to save or order by clicking the box next to the document, or click the link above the document to order directly.

save locally as: PDF document search strategy: do not include the search strategy

order

IEEE USPTO Full Text Retrieval Options

☑ **document 1 of 1** Order Document

INSPEC - 1969 to date (INZZ)

Accession number & update
4619820, B9404-1130B-068, C9404-7410D-159; 940309.

Title
Single-layer global routing.

Author(s)
Sarrafzadeh-M; Kuo-Feng-Liao; Wong-C-K.

Author affiliation
Dept of Electr Eng & Comput Sci, Northwestern Univ, Evanston, IL, USA.

Source
IEEE-Transactions-on-Computer-Aided-Design-of-Integrated-Circuits-and-Systems (USA), vol.13, no.1, p.38-47, Jan. 1994.

CODEN
ITCSDI.

ISSN
ISSN: 0278-0070, CCCC: 0278-0070/94/ ($04.00).

Publication year
1994.

Language
EN.

Publication type
J Journal Paper.

Treatment codes
P Practical; X Experimental.

Abstract
We introduce the single-layer global routing problem (SLGRP), also called homotopic routing or rubber-band-equivalent routing, and propose a technique for solving it. Given a set of nets, the proposed technique first determines the routing sequence based on the estimated **congestion,** the bounding-box length and priority. Then, it finds a routing **path,** being a sequence of tiles, for each net (one net at a time), avoiding "congested" areas. The overall goal of the algorithm is to maximize the number of routed nets. The proposed global router is the first true single-layer global router ever reported in the literature. The size of tiles, w*w, is an input parameter in our algorithm. For w=1, the proposed global router serves as an effective detailed router. An optimal postprocessing algorithm, minimizing wire length and number of bends, under homotopic transformation, is presented. The technique has been

implemented and tried out for randomly generated **data.** The algorithm is very efficient and produces good results. (37 refs).

Descriptors

circuit-layout-CAD; network-routing; VLSI.

Keywords

single layer global routing; SLGRP; homotopic routing; rubber band equivalent routing; routing sequence; **congestion map;** bounding box length; routing **path;** tile sequence; algorithm; routed net maximization; tile size; optimal postprocessing algorithm; wire length; homotopic transformation; VLSI layout; Density Algorithm.

Classification codes

```
B1130B    (Computer-aided circuit analysis and design).
B2570     (Semiconductor integrated circuits).
C7410D    (Electronic engineering).
```

Dial g DataStar

options | logoff | feedback | help

databases | easy search

Advanced Search:

INSPEC - 1969 to date (INZZ)

limit

Search history:

No.	Database	Search term	Info added since	Results	
1	INZZ	congestion ADJ map AND datapath	unrestricted	0	-
2	INZZ	congestion ADJ map AND data SAME path	unrestricted	1	show titles
3	INZZ	2 AND wire	unrestricted	1	show titles
4	INZZ	3 AND (math OR probability)	unrestricted	0	-

hide | delete all search steps... | delete individual search steps...

Enter your search term(s): Search tips ☐ Thesaurus mapping

whole document

Information added since: (YYYYMMDD) or: none

search

Select special search terms from the following list(s):

- Publication year
- Classification codes A: Physics, 0-1
- Classification codes A: Physics, 2-3
- Classification codes A: Physics, 4-5
- Classification codes A: Physics, 6
- Classification codes A: Physics, 7
- Classification codes A: Physics, 8
- Classification codes A: Physics, 9
- Classification codes B: Electrical & Electronics, 0-5
- Classification codes B: Electrical & Electronics, 6-9
- Classification codes C: Computer & Control
- Classification codes D: Information Technology

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	4	(congestion adj map) and datapath	USPAT	2005/10/18 12:58
2	BRS	L2	4	(congestion adj map) and datapath and I	USPAT	2005/10/18 12:58
3	BRS	L3	0	(congestion adj map) and datapath and IC	USPAT	2005/10/18 12:58
4	BRS	L4	3	(congestion adj map) and datapath and chip	USPAT	2005/10/18 12:59
5	BRS	L5	2	(congestion adj map) and datapath and chip and predetermined	USPAT	2005/10/18 13:04
6	BRS	L6	618	716/12.ccls.	USPAT	2005/10/18 13:15
7	BRS	L7	688	716/8.ccls.	USPAT	2005/10/18 13:15

Google Scholar BETA

wire probability datapath connections "conges Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar Results **1** - **2** of **2** for wire probability **datapath connections** "congestion map". (**0.07** seconds)

Tip: Try removing quotes from your search to get more results.

Benchmarking for Large-Scale Placement and Beyond
SN Adya, MC Yildiz, IL Markov, PG Villarrubia, PN ... - IEEE Transactions on Computer-Aided Design of Integrated ..., 2004 - ieeexplore.ieee.org
... In congestion-driven mode, Dragon behaves like a fixed-die placer and allocates white space according to an internal **congestion map**. **...**
Cited by 26 - Web Search - vlsicad.eecs.umich.edu - vlsicad.ucsd.edu - acm.org - all 17 versions »

Dear Associate Editor and Reviewers,
S Adya, M Yildiz, I Markov, P Villarrubia, P ... - eecs.umich.edu
... the **wire** length for an unroutable placement is completely useless. **...** like a fixed-die placer and allocates whitespace according to an internal **congestion map**. **...**
View as HTML - Web Search - eecs.umich.edu

wire probability datapath connection Search

Google Home - About Google - About Google Scholar

Google Scholar BETA "Alexaner Tetebaum" Search
Advanced Scholar Search
Scholar Preferences
Scholar Help

Did you mean: "***Alexander Tetenbaum***"

Your search - **"Alexaner Tetebaum"** - did not match any articles.

Suggestions:

- Make sure all words are spelled correctly.
- Try different keywords.
- Try more general keywords.
- Try your query on the entire web.

Google Home - About Google - About Google Scholar